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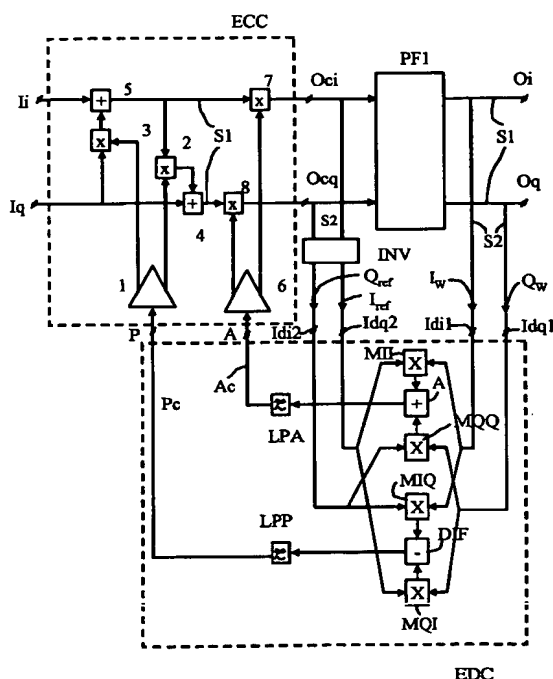
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(54) Title: **MIRROR SUPPRESSION CIRCUIT AND RECEIVER USING SUCH CIRCUIT**



(57) **Abstract:** Mirror suppression circuit and receiver using such mirror suppression circuit comprising a first quadrature signal path coupled between quadrature signal input and output terminals and including an error correction circuit for correction of amplitude and phase errors in a carrier modulated quadrature signal comprising a pair of in-phase and phase quadrature signal components. To obtain a suppression of both amplitude and phase imbalance of said carrier modulated quadrature signal as well as signal amplitude variations, a quadrature output of said error correction circuit being coupled through a first filter circuit for a selection of said quadrature signal to a first quadrature input of an error detection circuit, said first quadrature signal path being coupled prior to said first filter circuit through a second quadrature signal path to a second quadrature input of said error detection circuit, said error detection circuit detecting amplitude and phase errors and providing amplitude and phase control signals to amplitude and phase control inputs of said error correction circuit for a negative feed back of said amplitude and phase errors to said error correction circuit, said amplitude control signal varying with at least one of products $I_w \cdot I_{ref}$ and $Q_w \cdot Q_{ref}$ and said phase control signal varying with at least one of products $I_w \cdot Q_{ref}$ and $Q_w \cdot I_{ref}$, I_w and Q_w , respectively I_{ref} and Q_{ref} , representing the in-phase and phase quadrature signal components of said quadrature signal at the first quadrature input of the error detection circuit, respectively the in-phase and phase quadrature signal components of a quadrature reference signal occurring at the negative carrier frequency of said quadrature signal at the second quadrature input of the error detection